Amendments of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) A method of configuring a memory controller, said memory controller having a plurality of input/output pins, said method comprising:

informing said memory controller of a type of memory; and

configuring at least one of said pins to have a functionality in accordance with said type of memory, ~~each configured pins having selectable functionality including control, chip select, and clock functions~~ wherein functionalities selectable for said configuring include a chip select function and a clock function.

2. (original) The method of claim 1 wherein said type of memory is a buffered memory.

3. (original) The method of claim 1 wherein said type of memory is an unbuffered memory.

4. (original) The method of claim 1 wherein said configuring comprises configuring said functionality of said pin to a clock signal function.

5. (original) The method of claim 4 wherein said clock signal function is a differential clock signal function.

6. (original) The method of claim 1 wherein said configuring comprises configuring said functionality of said pin to a chip select signal function.

7. (original) The method of claim 1 wherein said functionality of said pin is one of a chip select signal and a clock signal.

8. (currently amended) A method of providing more than one function for an output pin of a memory controller, said method comprising:

providing a clock signal within said memory controller;

providing a ~~control~~ chip select signal within said memory controller;

selecting within said memory controller one of said clock signal and said ~~control~~ chip select signal based on a type of memory; and

coupling said selected signal to said output pin.

9. (original) The method of claim 8 wherein said type of memory is a buffered memory.

10. (original) The method of claim 8 wherein said type of memory is an unbuffered memory.

11. (original) The method of claim 8 wherein said clock signal is a differential clock signal.

12. (cancelled)

13. (currently amended) A memory controller comprising:

an output pin;

a multiplexer having two inputs, a control input, and an output coupled to said output pin;

a chip select signal coupled to one of said two inputs;

a ~~control~~ clock signal coupled to the other one of said two inputs; and

a control signal coupled to said control input that selects one of said chip select signal and said ~~control~~ clock signal based on a type of memory.

14. (original) The memory controller of claim 13 wherein said type of memory is a buffered memory.

15. (original) The memory controller of claim 13 wherein said type of memory is an unbuffered memory.

16. (cancelled)

17. (currently amended) The memory controller of claim [[16]] 13 wherein said clock signal is a differential clock signal.

Claims 18-22. (cancelled)

23. (currently amended) A memory controller comprising:

an output pin; and

circuitry coupled to said output pin that provides said output pin with ~~selectable functionality~~ a function selected in accordance with a type of memory, said ~~functionality including control,~~ circuitry operative to select one of at least a chip select[[,]] function and a clock ~~functions~~ function.

24. (currently amended) The memory controller of claim 23 wherein ~~said functionality of said output pin is one of a chip select signal and a clock signal~~ selection of the chip select function provides a chip select signal to said output pin; and

wherein selection of the clock function provides a clock signal to said output pin.

25. (currently amended) A memory circuit comprising:

a plurality of memory modules, said memory modules being of at least one type; and

a memory controller coupled to said memory modules via a plurality of pins, ~~each of~~ at least one of said pins having a selectable functionality based on said type of said memory modules, said ~~functionality including control,~~ memory controller operative to select a chip select[[,]] function and a clock ~~functions~~ function for each of said at least one of said pins having the selectable functionality.

26. (currently amended) The memory circuit of claim 25 wherein ~~said selectable functionality comprises~~ selection of the clock function provides a clock signal.

27. (currently amended) The memory circuit of claim 25 wherein ~~said selectable functionality comprises~~ selection of the clock function provides a chip select signal.

28. (currently amended) A computer system comprising:

a central processing unit;

a memory controller coupled to said central processing unit, said memory controller having a plurality of input/output pins; and

a plurality of memory modules of at least one type coupled to said memory controller via said pins; wherein:

each one of a subset of said pins has selectable functionality, said selectable functionality based on said type of said memory modules, said selectable functionality including ~~control,~~ a chip select[[,]] function and a clock ~~functions~~ function.

29. (currently amended) The computer system of claim 28 wherein said selectable functionality ~~comprises~~ is a clock ~~signal~~ function.

30. (currently amended) The computer system of claim 28 wherein said selectable functionality ~~comprises~~ is a chip select ~~signal~~ function.

31. (currently amended) Apparatus for configuring a memory controller, said memory controller having a plurality of input/output pins, said apparatus comprising:

means for informing said memory controller of a type of memory; and

means for configuring at least one pin of said memory controller to have a functionality in accordance with said type of memory, each of ~~pins~~ said at least one pin configurable by said means for configuring having selectable functionality including ~~control,~~ a chip select[[,]] function and a clock ~~functions~~ function.

32. (currently amended) Apparatus for providing more than one function for an output pin of a memory controller, said apparatus comprising:

means for providing a clock signal within said memory controller;

means for providing a ~~control~~ chip select signal within said memory controller;

means for selecting within said memory controller one of said clock signal and said ~~control~~ chip select signal based on a type of memory; and

means for coupling said selected signal to said output pin.

33. (currently amended) A memory controller comprising:

an output pin;

multiplexer means for outputting one of at least two signals to said output pin;

signal means for selecting a chip, said signal means for selecting coupled to said multiplexer means;

~~control~~ clock signal means coupled to said multiplexer means; and

means coupled to said multiplexer means for selecting one of said ~~control~~ signal means for selecting and said clock signal means based on a type of memory.

34. (currently amended) A memory controller comprising:

an output pin;

multiplexer means having two inputs, a control input, and an output coupled to said output pin;

a clock signal coupled to one of said two inputs;

a ~~control~~ chip select signal coupled to the other one of said two inputs; and

means coupled to said control input for selecting one of said clock signal and said ~~control~~ chip select signal based on a type of memory.

35. (currently amended) A memory controller comprising:

an output pin; and

means for providing said output pin with selectable functionality in accordance with a type of memory, said selectable functionality including ~~control,~~ a chip select[[,]] function and a clock ~~functions~~ function.

36. (currently amended) A memory circuit comprising:

a plurality of memory modules, said memory modules being of at least one type; and

memory controller means coupled to said memory modules via input/output means, one of said input/output means having a selectable functionality based on said type of said memory modules, said selectable functionality including ~~control,~~ a chip select[[,]] function and a clock ~~functions~~ function.

37. (currently amended) A computer system comprising:

central processing means;

memory controller means coupled to said central processing means, said memory controller means having a plurality of input/output means;

a plurality of memory modules of at least one type coupled to said memory controller means via said input/output means; wherein:

each one of a subset of said input/output means has selectable functionality, said selectable functionality based on said type of said memory modules and including ~~control,~~ a chip select[[,]] function and a clock ~~functions~~ function.